

REMARKS/ARGUMENTS

Claims 1-3 and 5-25 are pending in the application. By the Amendment, claims 1-3, 5, 6, 8-16, 18, and 19 are amended, and new claims 20-25 are added. It is believed no new matter is introduced in the application. Support for the claims can be found throughout the original specification, including the claims and the drawings originally filed. Reconsideration of the application in view of the above amendments and at least the reasons below is respectfully requested.

The Office Action, at page 2, rejects claims 2, 5, 13, and 16 under 35 U.S.C. § 112, second paragraph. Applicant respectfully traverses the rejection and submits that grounds for the rejection are obviated by the above amendments to the claims. Withdrawal of the rejection is thus respectfully requested.

The Office Action, also at page 2, rejects claims 1, 2, 5, 7, 12, 13, and 16-19 under 35 U.S.C. § 102(e) over U.S. Patent No. 6,763,478 to Bui. The Office Action, at page 3, rejects claims 3, 4, 6, 8-11, 14, and 15 under 35 U.S.C. § 103(a) over Bui. Because Bui fails to disclose or suggest all the features of the claims, the rejections are respectfully traversed.

With respect to claims 1-11, Applicant respectfully submits that amended claim 1 is directed to an apparatus having a CPU, that includes features of a clock generator generating a first clock signal for the CPU, and a second clock signal, wherein the first and second clock signals are two distinct clock signals outputted by the clock generator and have different frequencies; and a bridge controller comprising a logic device for adjusting the second clock

signal based on a power source and independent of the first clock signal. Applicant respectfully submits that at least such features and combinations thereof are not disclosed or suggested by Bui.

Applicant respectfully submits that Bui relates to a computer system in which a clock generator 50 provides either a high performance or a low performance clock signal depending upon whether power supplied to the computer system is DC or AC power. (Bui at column 4, line 65 – column 5, line 2). As shown in Figure 2 of Bui, and at column 5, lines 2-36, the same high (i.e., 100 MHz) or low (i.e., 66 MHz) clock signal outputted from the clock generator 50 as a front side bus (FSB) clock 65, is sent to both the north bridge ASIC 30 and the CPU 71 to determine the clock frequency of the FSB 105 and the memory bus 95. Accordingly, Bui provides that the frequencies of both the FSB 105 bus and the memory bus 95 will be set to 66 MHz in low performance mode, and to 100 MHz in high performance mode. Thus, Bui does not disclose or suggest that first and second clock signals are two distinct clock signals outputted by the clock generator and have different frequencies and combinations thereof as recited in claim 1. Therefore, claim 1 defines patentable subject matter.

For at least the above reasons, Applicant respectfully submits that claim 1 is allowable. Claims 2, 3, and 5-11 ultimately depend from claim 1, and thus are allowable for at least the same reasons, as well as additional patentable features recited therein and the combinations thereof. Withdrawal of the rejections is thus respectfully requested. Claim 4 is canceled and the rejection thereof is therefore moot.

With respect to claims 12-18, Applicant respectfully submits that amended independent claim 12 is directed to an apparatus having a CPU and a bridge controller, that includes features of a clock generator generating a first clock signal; and a clock adjuster receiving the first clock signal and operating in a power source mode, the clock adjuster generating a second clock signal for the CPU and a third clock signal for the bridge controller, wherein the second and third clock signals are two distinct clock signals outputted by the clock adjuster and have frequencies that are independent of each other. Applicant respectfully submits that at least such features and combinations thereof are not disclosed or suggested by Bui.

As discussed above with respect to claim 1, Applicant respectfully submits Bui provides that the clock generator 50 itself outputs an FSB clock 65 signal having a single frequency (i.e., either 66 or 100 MHz) that is sent to both the north bridge ASIC 30 and the CPU 71 to determine the clock frequency of the FSB 105 and the memory bus 95. Thus, Applicant respectfully submits that Bui fails to disclose or suggest a clock adjuster receiving the first clock signal and generating a second clock signal for the CPU and a third clock signal for the bridge controller, wherein the second and third clock signals are two distinct clock signals outputted by the clock adjuster and have frequencies that are independent of each other. Therefore, claim 12 defines patentable subject matter.

For at least the above reasons, Applicant respectfully submits that claim 12 is allowable. Claims 13-18 ultimately depend from claim 12, and thus are allowable for at least the same

Serial No. 10/003,345
Amdt. Dated October 26, 2004
Reply to Office Action of July 26, 2004

Docket No. LT-0006

reasons, as well as additional patentable features recited therein and the combinations thereof.

Withdrawal of the rejections is thus respectfully requested.

With respect to independent claim 19, Applicant respectfully submits that claim 19 is allowable for reasons similar to claims 1 and 12, as well as additional patentable features recited therein and the combinations thereof. Withdrawal of the rejection is thus respectfully requested.

In addition, Applicant respectfully submits newly added claims 20-25 define patentable subject matter for similar reasons as discussed above.

Serial No. 10/003,345
Amdt. Dated October 26, 2004
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Docket No. LT-0006

CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney, **Garth D. Richmond**, at the telephone number listed below. Favorable consideration and prompt allowance are earnestly solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
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